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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,911	03/26/2004	Mehdi Kazemi-Nia	1020.P18339	6318

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EXAMINER	
LE, THI Q	
ART UNIT	**PAPER NUMBER**
2613	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,911	KAZEMI-NIA ET AL.	
	Examiner	Art Unit	
	Thi Q. Le	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,12-14 and 16-20* is/are rejected.

7)☐ Claim(s) *6, 11, 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/26/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) filed on 3/26/2004 was considered by the examiner.

Drawings

2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office Action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended". If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office Action. If a response to the present Office Action fails to include proper drawing corrections, corrected drawings or arguments therefor, the response can be held **NON-RESPONSIVE** and/or the application could be **ABANDONED** since the objections/corrections to the drawings are no longer held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "**110**" has been used to designate both **the optical transceiver unit** and **the amplifiers**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

a) In **paragraph 0014**, replace "**laser 160**", with **--laser 150--**, after "in this manner".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. **Claims 1-5, 7-10, 12 and 16-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bostak et al. (US Patent # 6,707,589)** in view of **Nguyen et al. (US PGPub 2004/0189388)**.

Consider **claim 1**, Bostak et al. clearly disclose, a driver circuit, comprising: a first driver circuit (read as, drive circuit 10; figure 1) having a first output terminal operatively responsive to an output load resistance corresponding to a modulator circuit (read as, the output terminal which is connected to resistor 14 and EAM 12; figure 1) and a second output terminal operatively responsive to a termination resistance (read as, output terminal which is connected to resistor 16; figure 1), said first driver circuit having a constant current source configured to supply a current

signal in response to an input signal applied to said first driver circuit (read as, Vin and Vin* input signals are connected to the gate of the transistor pair 11; and DC current source I_D is connected to the source of transistor pair 11; figure 1) (figure 1, column 1 lines 35-60). Bostak et al. fails to disclose, a second driver circuit having a constant current source, said second driver circuit operatively responsive to said first driver circuit by a first and second input terminals.

In related art, Nguyen et al. disclose a series of differential amplifier connected in parallel to each other. Wherein, the differential amplifiers have identical circuit structure as the driver circuit disclosed in Applicant's specification figures 2-3. Further, Nguyen et al. show, a second driver circuit having a constant current source, said second driver circuit operatively responsive to said first driver circuit by a first and second input terminals (read as, each differential amplifier 3603 has a separate current source 3605 (i.e. first, second, third... etc. driver circuits have a separate current source connected to it), and wherein each amplifier 3603 receives input signal from the gate of the transistor pair) (figure 36, paragraph 0475-0476).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Nguyen et al. with Bostak et al. Since add additional drive circuits parallel to each other, provides the ability to change the output signal level. Thus increasing the operating range of the drive circuit.

Consider **claim 2**, and **as applied to claim 1 above**, Bostak et al. as modified by Nguyen et al. disclosed that each current source 3605 can be individually turn on and off; thus disabling or enable the differential amplifier circuit 3603 (Nguyen et al., paragraph 0476). But fails to disclose, wherein said constant current source of said second driver circuit is disabled.

It would have been obvious for a person of ordinary skill in the art at the time of the invention to understand, since each amplifier circuit 3603 can be disable or enable based on the on/off state of the current source 3605. Then based on the desired output signal level, each individual amplifier circuit 3603 can be enabled or disabled; thus, if the a certain output signal level is desired the second amplifier circuit 3603 (i.e. second driver circuit) can be disable to attain the desired output signal level (Nguyen et al., figure 36).

Consider **claim 3**, and **as applied to claim 1 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said first driver circuit further comprises a first transistor (read as, the right transistor of the transistor pair 11; Bostak et al., figure 1), said first transistor having a source terminal operatively responsive to said constant current source (read as, source terminal of said right transistor is connected to DC current source I_D; Bostak et al., figure 1), a drain terminal operatively responsive to a first resistor (read as, drain terminal of said right transistor is connected to resistor R_2; figure 1), and a gate terminal configured to receive said input signal (read as, gate terminal of said right transistor is connected input signal Vin*; Bostak et al., figure 1).

Consider **claim 4**, and **as applied to claim 3 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said input signal is a first input signal (read as, input signal Vin*; Bostak et al., figure 1), said first driver circuit further comprising a second transistor (read as, the left transistor of the transistor pair 11; Bostak et al., figure 1) having a source terminal operatively responsive to said constant current source, and said source terminal of said first transistor (read as, source terminal of said left transistor is connected to DC current source I_D; Bostak et al., figure 1), a drain terminal operatively responsive to a second resistor (read as, drain

terminal of said right transistor is connected to resistor R_2; Bostak et al., figure 1) and a gate terminal configured to receive a second input signal (read as, gate terminal of said right transistor is connected input signal Vin*; Bostak et al., figure 1).

Consider **claim 5**, and **as applied to claim 4 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said first output terminal is connected, at a first end, to said drain terminal of said first transistor and to an input of said modulator circuit at a second end (read as, output terminal of said right transistor is connected from its drain to resistor 14 and EAM 12; Bostak et al., figure 1), and said second output terminal is connected, at a first end, to said drain terminal of said second transistor and to said termination resistance at a second end (read as, output terminal of said left transistor is connected from its drain to resistor 16; Bostak et al., figure 1).

Consider **claim 7**, and **as applied to claim 1 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said second driver circuit further comprising a first transistor (read as, right transistor of the transistor pair of amplifier circuit 3603; Nguyen et al., figure 36), said first transistor having a source terminal operatively responsive to said constant current source (read as, source terminal of said right transistor is connected to current source 3605; Nguyen et al., figure 36), a drain terminal operatively responsive to a first resistor (read as, source terminal of said right transistor is connected to a resistor; Nguyen et al., figure 36), and a gate terminal configured to receive said input signal (read as, source terminal of said right transistor is connected to an input signal; Nguyen et al., figure 36) (note, the input signals are Vin and Vin* as disclosed by Bostak et al. figure 1; and wherein each amplifier circuit 3603, disclose by Nguyen et al. figure 36, receives the same input signals).

Consider **claim 8**, and **as applied to claim 7 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said input signal is a first input signal (read as, input signal Vin*; Bostak et al., figure 1), and said second driver circuit further comprising a second transistor (read as, left transistor of the transistor pair of amplifier circuit 3603; Nguyen et al., figure 36) having a source terminal operatively responsive to said constant current source of said second driver circuit and said source terminal of said first transistor (read as, source terminal of said left transistor is connected to current source 3605; Nguyen et al., figure 36), a drain terminal operatively responsive to a second resistor (read as, source terminal of said right transistor is connected to another resistor; Nguyen et al., figure 36) and a gate terminal configured to receive a second input signal (note, since Bostak et al. figure 1, disclose the gate of the right and left transistor of transistor pair 11 receives input signals Vin* and Vin, respectively; and Nguyen et al. figure 36 disclosed, each amplifier circuit 3603 receives the same input signals. It would have been obvious that when the teaching of Nguyen et al. as applied with the teaching of Bostak et al. there would be a plurality of drive circuits 10 and each drive circuit receives input signals Vin* and Vin at its the gate of the right and left transistor of transistor pair 11, respectively).

Consider **claim 9**, and **as applied to claim 8 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said second driver circuit further comprising first and second output terminals (read as, output 3506; Nguyen et al., figure 36), said first output terminal connected at a first end to said drain terminal of said second transistor and to said termination resistance at a second end, said second output terminal connected at a first end to said drain terminal of said first transistor and to an input of said modulator circuit (note, Nguyen et al. shows that the first outputs from all amplifier circuits 3603 are connected together, and the

second outputs are also connected together. Thus, when teaching of Nguyen et al. is applied with the teaching of Bostak et al., there would be a plurality of drive circuits 10; wherein the first outputs (i.e. the output from drain of right transistor of transistor pair 11) of all drive circuits are connected to resistor 14 and EAM 12 and second outputs (i.e. the output from drain of left transistor of transistor pair 11) of all drive circuits are connected to resistor 16).

Consider **claim 10**, and **as applied to claim 1 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said first driver circuit further comprising first and second power supply terminals, said second driver circuit further comprising first and second power supply terminals (read as, all amplifier (i.e. first, second, third... etc. drive circuit) circuits 3603 are connected to two power supply terminal Vdd, as shown by Nguyen et al., figure 36), said first driver circuit further operatively responsive to said second driver circuit by said first and second output terminals (note, based on the enable and disable state of each amplifier circuit 3603, the output level on output 3506 changes; Nguyen et al., paragraph 0476).

Consider **claim 12**, and **as applied to claim 1 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said first and second driver circuits are mirror images of each other (read as, all amplifier circuit 3603 are identical to each other; Nguyen et al., figure 36).

Consider **claim 16**, Bostak et al. clearly disclose, a method, comprising: supplying input signals to first modulator driver circuit (read as, supplying input signals Vin and Vin* to drive circuit 10; figure 1), said circuits including a constant current source (read as, DC current source I_D; figure 1); connecting a first output from said first modulator driver circuit to said optical modulator (read as, the output terminal which is connected to resistor 14 and EAM 12; figure 1);

connecting a second output from said first modulator driver circuit to a termination resistance (read as, output terminal which is connected to resistor 16; figure 1) (figure 1, column 1 lines 35-60). Bostak et al. fail to disclose, a second driver circuit including a constant current source and shutting off said current source included in said second modulator driver circuit.

In related art, Nguyen et al. disclose a series of differential amplifier connected in parallel to each other. Wherein, the differential amplifiers have identical circuit structure as the driver circuit disclosed in Applicant's specification figures 2-3. Further, Nguyen et al. show, a second driver circuit having a constant current source (read as, each differential amplifier 3603 has a separate current source 3605 (i.e. first, second, third... etc. driver circuits have a separate current source connected to it), and wherein each amplifier 3603 receives input signal from the gate of the transistor pair) (figure 36, paragraph 0475-0476).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Nguyen et al. with Bostak et al. Since add additional drive circuits parallel to each other, provides the ability to change the output signal level. Thus increasing the operating range of the drive circuit.

Further, It would have been obvious for a person of ordinary skill in the art at the time of the invention to understand, since each amplifier circuit 3603, as shown by Nguyen et al. figure 36, can be disable or enable based on the on/off state of the current source 3605. Then based on the desired output signal level, each individual amplifier circuit 3603 can be enabled or disabled; thus, if the a certain output signal level is desired the second amplifier circuit 3603 (i.e. second driver circuit) can be disable to attain the desired output signal level (Nguyen et al., figure 36).

Consider **claim 17**, and **as applied to claim 16 above**, Bostak et al. as modified by Nguyen et al. further disclose, wherein said first and second driver circuits are mirror images of each other (read as, all amplifier circuit 3603 are identical to each other; Nguyen et al., figure 36).

Consider **claim 18**, and **as applied to claim 16 above**, Bostak et al. as modified by Nguyen et al. further disclose, connecting a first output (read as, outputs 3506; Nguyen et al., figure 36) of said second modulator driver circuit to said termination resistance; and connecting a second output (read as, outputs 3506; Nguyen et al., figure 36) of said second modulator driver circuit to said optical modulator (note, Nguyen et al. shows that the first outputs from all amplifier circuits 3603 are connected together, and the second outputs are also connected together. Thus, when teaching of Nguyen et al. is applied with the teaching of Bostak et al., there would be a plurality of drive circuits 10; wherein the first outputs (i.e. the output from drain of right transistor of transistor pair 11) of all drive circuits are connected to resistor 14 and EAM 12 and second outputs (i.e. the output from drain of left transistor of transistor pair 11) of all drive circuits are connected to resistor 16).

Consider **claim 19**, and **as applied to claim 16 above**, Bostak et al. as modified by Nguyen et al. further disclose, supplying power to said first modulator driver circuit such that a constant current source included in said first modulator driver circuit operates to provide a signal to said optical modulator and said termination resistance (Bostak et al. figure 1, column 1 lines 35-60); but fail to disclose, shutting off power supplied to said second modulator driver circuit.

It would have been obvious for a person of ordinary skill in the art at the time of the invention to understand, since each amplifier circuit 3603, as shown by Nguyen et al. figure 36,

can be disable or enable based on the on/off state of the current source 3605. Then based on the desired output signal level, each individual amplifier circuit 3603 can be enabled or disabled; thus, if the a certain output signal level is desired the second amplifier circuit 3603 (i.e. second driver circuit) can be disable to attain the desired output signal level (Nguyen et al., figure 36).

Consider **claim 20**, and **as applied to claim 19 above**, claim 20 is rejected for the same reason as claim 18 above.

9. **Claims 13-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Taylor (US Patent # 6,256,127)** in view of **Bostak et al. (US Patent # 6,707,589)** and further in view of **Nguyen et al. (US PGPub 2004/0189388)**.

Consider **claim 13**, Taylor clearly discloses, an optical communication system, comprising: a transmission medium configured to allow propagation of optical signals (read as, optical waveguide 60; figure 2); at least one optical amplifier disposed along said transmission path for amplifying said optical signals (read as, optical amplifier 70; figure 2); and a transceiver (read as, transponder 30, also used as remodulator 130, figures 1 and 2) operatively responsive to said transmission medium, said transceiver comprising a light source (read as, laser 36; figure 1), a modulator (read as, modulator 38; figure 1) for modulating said information signals onto light signals generated by said light source and a modulator driver (read as, modulator driver 39; figure 1) for supplying electrical signals representing said information signals to said modulator. Taylor fails to disclose, said modulator driver comprising a first driver circuit having a first output terminal operatively responsive to an output load resistance corresponding to said modulator circuit and a second output terminal operatively responsive to a termination resistance, said first driver circuit having a constant current source configured to supply a current

signal in response to an input signal applied to said first driver circuit and a second driver circuit having a constant current source, said second driver circuit operatively responsive to said first driver circuit by a first and second input terminals.

In related art, Bostak et al. disclose, an optical modulator drive circuit. Wherein, said modulator driver comprising a first driver circuit (read as, drive circuit 10; figure 1) having a first output terminal operatively responsive to an output load resistance corresponding to a modulator circuit (read as, the output terminal which is connected to resistor 14 and EAM 12; figure 1) and a second output terminal operatively responsive to a termination resistance (read as, output terminal which is connected to resistor 16; figure 1), said first driver circuit having a constant current source configured to supply a current signal in response to an input signal applied to said first driver circuit (read as, Vin and Vin* input signals are connected to the gate of the transistor pair 11; and DC current source I_D is connected to the source of transistor pair 11; figure 1) (figure 1, column 1 lines 35-60).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Bostak et al. with Taylor. Since Bostak et al. show common circuitry of a typical modulator drive circuit; which includes differential amplifiers, DC current source, and resistors.

In related art, Nguyen et al. disclose a series of differential amplifier connected in parallel to each other. Wherein, the differential amplifiers have identical circuit structure as the driver circuit disclosed in Applicant's specification figures 2-3. Further, Nguyen et al. show, a second driver circuit having a constant current source, said second driver circuit operatively responsive to said first driver circuit by a first and second input terminals (read as, each differential

amplifier 3603 has a separate current source 3605 (i.e. first, second, third... etc. driver circuits have a separate current source connected to it), and wherein each amplifier 3603 receives input signal from the gate of the transistor pair) (figure 36, paragraph 0475-0476).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to incorporate the teachings of Nguyen et al. with Taylor modified by Bostak et al. Since add additional drive circuits parallel to each other, provides the ability to change the output signal level. Thus increasing the operating range of the drive circuit.

Consider **claim 14**, and **as applied to claim 13 above**, Taylor modified by Bostak et al. and further modified by Nguyen et al. further disclose, wherein said first driver circuit further comprising first and second power supply terminals, said second driver circuit further comprising first and second power supply terminals (read as, all amplifier (i.e. first, second, third... etc. drive circuit) circuits 3603 are connected to two power supply terminal Vdd, as shown by Nguyen et al., figure 36), said first driver circuit further operatively responsive to said second driver circuit by said first and second output terminals (note, based on the enable and disable state of each amplifier circuit 3603, the output level on output 3506 changes; Nguyen et al., paragraph 0476).

Allowable Subject Matter

10. **Claims 6, 11 and 15** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Main, W. Eric; 4,109,214

b) Stilwell et al.; 5,224,111

c) Wong, Thomas Y.; 5,550,513

d) Navabi et al.; 5,585,763

f) Imai et al.; 5,706,117

g) Takahashi, Hiroyuki; 5,900,745

h) Kimura, Madoka; 2003/0011865

i) Pobanz, Carl Walter; 6,836,185

j) Martin, Chris G.; 2006/0109723

l) Watanabe et al.; 7,099,596

m) Cox et al.; 7,164,692

n) Komatsubara et al.; 5,546,218

o) Turudic et al; 2003/0006842

p) Chujo et al.; 6,606,177

r) Umeda et al.; 2004/0075474

s) Aemireddy, Arvind Reddy; 2005/0099748

12. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thi Le whose telephone number is (571) 270-1104. The Examiner can normally be reached on Monday-Friday from 7:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Thi Le

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER